determine whether a recording/reproducing apparatus is in a recording mode or a reproducing mode of operation (see Office Action page 2, first sentence of second to last paragraph, and sentence bridging pages 2 and 3). However, the Final Rejection acknowledges, in light of Applicant's remarks presented in response to the Office Action, that Applicant's disclosure does enable a skilled artisan to understand how the bit signals are compared for determining the mode of operation of the recording/reproducing apparatus (see Final Rejection page 2, lines 2-6 of first paragraph). Therefore, the basis for the rejections applied in the previous Office Action has been overcome.

The Final Rejection states that the basis for the present rejections is that a skilled artisan would not understand from Applicant's disclosure how CPU 115 in Fig. 1 could receive the bit signals for their comparison (Final Rejection page 2, lines 9-14 of first paragraph). This basis for rejecting the claims was not set forth in the Office Action, and Applicant has not been provided an opportunity to respond to the new basis prior to issuance of this final rejection. Since this new basis for rejecting the claims was not necessitated by an amendment of the claims, the finality of the rejections is premature. Therefore,

withdrawal of the final status of the office action is warranted (see MPEP §706.07(a) second paragraph, first sentence).

Regarding the new basis for rejecting the claims, the Applicant traverses based on the following remarks.

The Final Rejection proposes that Applicant's disclosure would not enable a skilled artisan to determine how CPU 115 in Fig. 1 could compare two bit signals (Final Rejection page 2, lines 11-13). The Final Rejection acknowledges that: (1) CPU 115 receives a bit signal identified in Fig. 1 as a reproduction input signal (page 2, lines 13-14 of first paragraph) and (2) Applicant's disclosure enables a skilled artisan to compare two signals with a CPU (page 2, lines 5-6 of first paragraph). Therefore, the only piece of information the Final Rejection proposes is missing from Applicant's disclosure is the manner by which CPU 115 obtains another signal to compare to the reproduction input signal.

However, the Applicant's specification discloses that a CPU 115 sets a bit signal (specification page 6, lines 16-17). Additionally, the specification discloses that the signal set by CPU 115 is compared with another signal output by a recording/reproducing apparatus 118 (page 7, lines 20-22), which other signal the Final Rejection acknowledges is received by CPU 115 and identifies as the reproduction input signal. Also, the

specification discloses that CPU 115 makes the comparison (page 7, line 1). Therefore, the Applicant's specification makes clear that CPU 115 compares a signal that it has set with a received signal.

The Final Rejection's conclusion that CPU 115 must necessarily receive a signal from a synthesizing portion 111, for comparison with the reproduction input signal, is unfounded (see Final Rejection page 2, lines 9-10 of first paragraph). The basis for this conclusion, asserted in the Final Rejection, is that Applicant discloses "the detected bit signal is compared with the multiplexed bit signal (multiplexed by synthesizing portion 111)" (see Final Rejection page 2, lines 7-9 of first paragraph).

However, the *detected bit signal*, referenced by the Final Rejection on page 2, lines 7-9, is the same signal the Final Rejection identifies as the reproduction input signal, in lines 13-14. And this signal is compared with a bit signal that synthesizing portion 111 multiplexes with a video signal output by encoder 109. According to standard English grammar, a bit signal that is multiplexed may properly be referred to as a multiplexed bit signal, and *vice versa*. From this it follows that "the multiplexed bit signal" is the bit signal that is

multiplexed by synthesizing portion 111 and this bit signal is compared to the detected bit signal.

Although the Final Rejection indicates Applicant's disclosure is ambiguous, there is no ambiguity as is apparent from an evaluation of the context in which the description is presented. The Final Rejection asserts the language "the multiplexed bit signal" is ambiguous. However, when this phrase is viewed in the context of Applicant's entire disclosure, the meaning is clear, for the reasons discussed above. The cited phrase from Applicant's disclosure refers to a bit signal that will be multiplexed by synthesizing portion 111.

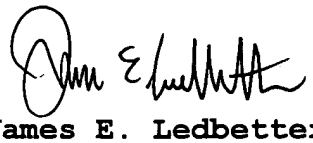
Accordingly, Applicants submit that one of ordinary skill in the art would understand, from the context of the Applicant's entire disclosure, how CPU 115 compares a received signal with one that CPU 115 has established. As a result, the Applicant's disclosure satisfies the requirements set forth in 35 USC §112, first paragraph, for the subject matter defined by claims 1-20. Therefore, allowance of claims 1-20 is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone

the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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